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14. ABSTRACT

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Abstract

In this project, we have demonstrated five new approaches to reduce the access resistances in GaN HEMTs in order to improve their RF performance. The first approach is based on strain engineering. Additive tensile biaxial strain has been introduced into an AlGaN/GaN hetero-structure grown on a Si wafer by reducing the thickness of the Si substrate after the growth of the nitride epilayer. As a result, the electron sheet density increases by ~25% and reaches n_s~1x10^{13} cm^{-2}. This intrinsic piezoelectric-induced doping allows decreasing the access resistance of AlGaN/GaN HEMTs. This new substrate-etching technology has been used to increase the on-current in the linear region and the current density of AlGaN/GaN transistors grown on silicon by 27%. The four others methods developed to reduced the access resistances are based on different recessed ohmic techniques. First, a new ohmic technology based on Si/Ge/Ti/Al/Ni/Au has been developed and it has allowed us to reduce both ohmic contact resistance by 55 % and surface roughness by 83 % with respect to conventional non-recessed Ti/Al/Ni/Au ohmic contacts. Using this metallization, the contact resistance has been decreased down to R_c~0.15 Ω.mm, which is one of the lowest contact resistance reported in the AlGaN/GaN literature. A second technology to reduce the contact resistance is based on the top-down fabrication of AlGaN/GaN nano-ribbons to allow the ohmic metal to contact the 2DEG directly. Lower R_c is observed in AlGaN/GaN NRs compared to the conventional planar device. The third approach is based on Si implantation of the access regions in InAlN/GaN structures. When this ion implantation is combined with recess ohmics, a low contact resistance of 0.04 Ω.mm was achieved, the lowest ever reported in InAlN/GaN structures. Finally, the development of a Au-free ohmic contact technology based on a Ti/Al/W metallization enables the fabrication of GaN-based transistors in Si fabs.

Introduction

High Electron Mobility Transistors (HEMTs) based on wide-bandgap III-V nitride hetero-structures have surpassed the performance of other competing material technologies in high-power performance at RF frequencies. For example, output power densities as high as 10.5 W/mm have been achieved at 40 GHz, far higher than that achievable in any other existing semiconductor technology. Furthermore, the high frequency performance of $Al_xGa_{1-x}N$/GaN HEMTs has rapidly increased in the recent years. For instance, transistors with current-gain cut-off frequencies (f_T) above 225 GHz and power-gain cut-off frequencies (f_{max}) of more than 300 GHz have been reported [1], which enables the use of these devices in power amplifiers for mm-wave applications. The high frequency performance of nitride HEMTs allow to compete and possibly replace not only other HEMT technologies, but also the bulky non-solid state vacuum tube-based devices such as traveling wave tubes that still deliver significant RF power at frequencies exceeding 100 GHz. This potential makes these devices based on nitride semiconductors extremely attractive for multiple military and civil applications in the mm-wave frequency range such as wideband wireless communication, anti-collision car radar systems and satellite transponders (Figure 1).

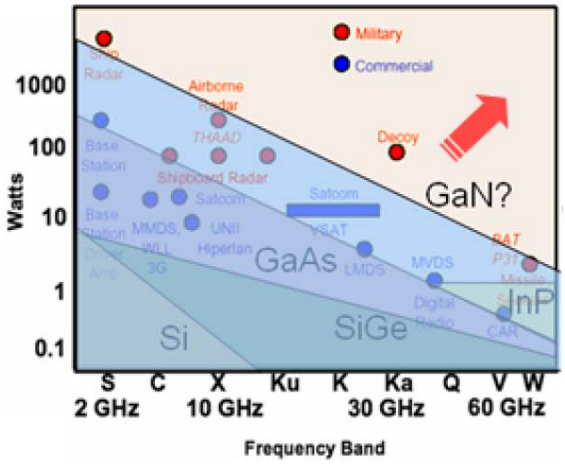


Figure 1. Some of the main potential applications for AlGaN/GaN power amplifiers at mm-wave frequencies.

In spite of these excellent results, the frequency performance of these transistors is still far from their theoretically limit and remains lower than the results reported by competing material such as InGaAs/GaAs HEMTs. To increase the frequency performance of GaN devices, the parasitic delays associated to the access resistances need to be drastically reduced.

The operating frequency of a HEMT is inversely proportional to the total delay of the carriers across the transistor (τ_{total}). This delay can be divided in three different components: intrinsic delay (τ_{int}), channel charging delay ($\tau_{channel}$), and drain delay (τ_{drain}). τ_{int} is the time taken by the electrons to cross the channel region under the gate, $\tau_{channel}$ is the time needed to charge and discharge the parasitic capacitances, and τ_{drain} is the time required by the electrons to cross the depletion region induced at the drain side of the gate. As shown in Figure 2, to improve the frequency performance of nitride HEMTs (i.e. to reduce the total delay) it is necessary to reduce all three parasitic delays. If we incorporate the access parasitic resistances (i.e. from the source and drain contacts to the channel), the expression for f_T becomes:

$$f_T = \frac{g_m/(2\pi)}{\left[C_{gs}+C_{gd}\right]\times\left[1+(R_s+R_d)/R_{ds}\right]+C_{gd}g_m(R_s+R_d)}$$

In the expression above, g_m is the transconductance, C_{gs} is the gate-source, capacitance and C_{gd} is the gate-drain capacitance, R_s is the source parasitic resistance, R_d is the drain parasitic resistance and R_{ds} is the output resistance of the transistor. We can also rewrite the expression for f_T in the following manner in order to better see the intrinsic and the parasitic delays

intrinsic delay parasitic delay

$$\frac{1}{2\pi f_T} = \frac{C_{gs}+C_{gd}}{g_m} + \frac{(C_{gs}+C_{gd})(R_s+R_d)}{g_m R_{ds}} + C_{gd}(R_s+R_d)$$

Due to these parasitic delays, the f_T's of transistors, especially deeply scaled transistors, are lower than what can be expected based on the intrinsic performance. In particular for GaN based HEMTs, the access resistances are higher than for HEMTs fabricated in other material systems (and C_{gd} is also higher for the same voltage due to high carrier concentrations). Figure 2 shows the predicted frequency performance for a GaN-based HEMT with a gate length of 50 nm and it shows that reducing access resistances significantly improves both f_{max} and f_T. Reducing the access resistances also lowers the knee voltage (the drain voltage at which the transistor transitions between the linear region and the saturation region for a fixed gate voltage). By lowering the knee voltage, higher on-currents can be achieved at lower drain voltages, which improves efficiency and reduces the electric field present in the drain access region. High electric fields in the drain access region induce depletion regions, thus contributing to drain delay. As shown in Figure 3, drain delay is a dominant component of the total delay in very short gate length transistors. Therefore, lower access resistances will allow for reducing the drain voltage without sacrificing current density, which in turn will reduce the drain delay and improve frequency performance.

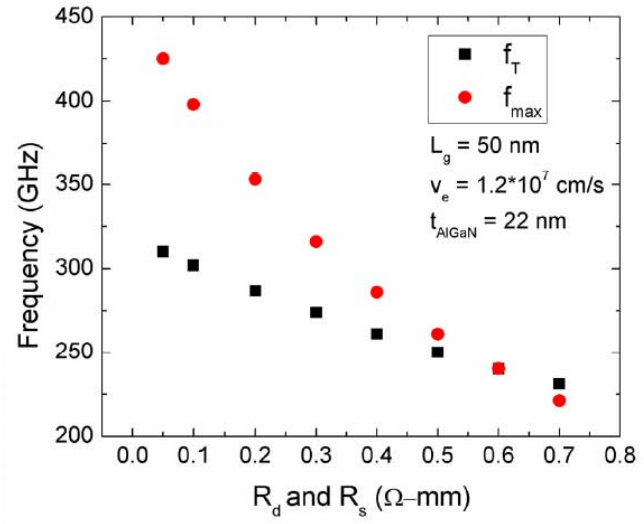


Figure 2: Frequency performance vs source and drain resistance. The on-current is assumed to be constant.

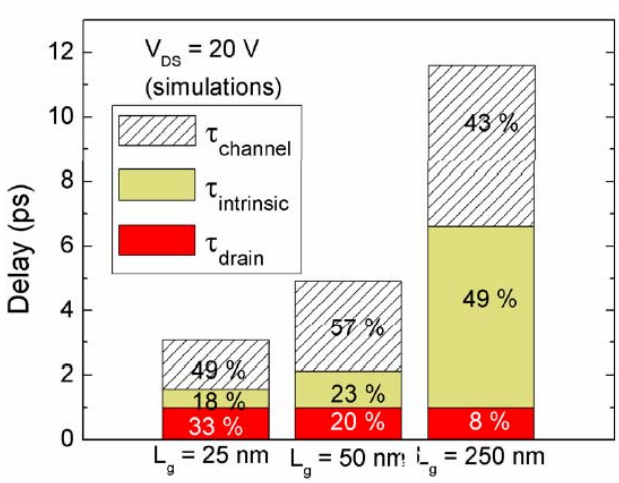


Figure 3: Various delays associated with transistor performance. Drain delay gets more dominant as gate lengths scale down.

In this project, we have focus our work on developing new technologies to reduce the access resistance in deep-submicron GaN HEMTs. We have demonstrated five new technologies, which we have studied in the five tasks in which we have divided this project:

- Task 1.- Use of strain engineering to reduce access resistances.
- Task 2.- New ohmic metal stack for ultra-low resistance.
- Task 3.- Advanced Recessed Ohmic Technology.
- Task 4.- Nano-ribbon fabrication for reduced contact resistances.
- Task 5.- Si implantation of InAlN/GaN structures.

Task 1: Use of strain engineering to reduce access resistances

Spontaneous (P_{sp}) and piezoelectric polarizations (P_z) in Nitrides are responsible for the very large two electron dimensional gas (2DEG) commonly observed at the AlGaN/GaN interface [2]. The P_z effect (or strain effect) on the AlGaN top layer by using SiN cap layer or increasing the Al content increase the charge density (ns) in AlGaN/GaN heterostructure.

In this work, we have investigated the effect of substrate-induced strain in the transport properties of AlGaN/GaN heterostructures grown on Si(111) substrates. Until now, the study of the effect of the substrate on the strain in the nitride epilayer has been challenging, as different substrates require completely different growth conditions and it is therefore difficult to decouple the effects of the substrate from the growth conditions. To overcome this growth challenge, we have used a new technology based on the backside substrate etching of AlGaN/GaN HEMT structures grown on a Si(111). By controlling the amount of remaining Si substrate, we can change the biaxial strain in AlGaN/GaN, study its effect in the transport properties of the 2DEG, and use it to reduce the access resistance in GaN-based transistors.

Room temperature Raman spectroscopy and Hall-Van Der Pauw measurements have been then performed on AlGaN/GaN with different thicknesses of remaining Si(111) substrate. An increase of n_s and mobility has been observed [3]. Changes in tensile biaxial strain are linearly related to the sheet carrier concentration in the 2DEG (n_s) by the following relationship [4]: $dn_s/d\varepsilon_{xx} \sim(2.5 \pm 0.5)\times10^{15}\ e^-/cm^2$ (1). Figure 4 shows the 2DEG carrier density measured by RT Hall-Van Der Pauw in our devices (solid line), and the 2DEG density predicted by equation (1) (dashed line). As expected, n_s increases quasi-linearly with the additional tensile strain induced by the substrate thickness reduction. n_s is enhanced by ~25% for the AlGaN/GaN sample with a Si substrate thickness of ~350 μm. These results agree well with the ones reported in Ref. 4, where the tensile stress of an AlGaN/GaN HEMT was changed externally through a bending apparatus.

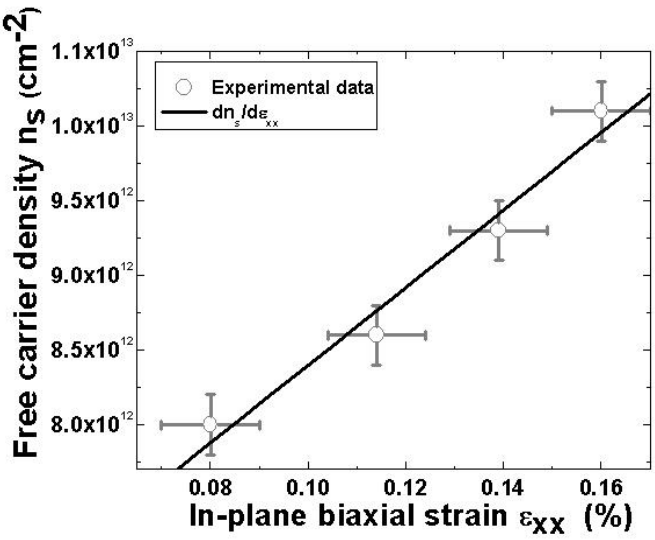


Figure 4. Room temperature free carrier density versus in-plane strain in AlGaN/GaN heterostructures as a function of remaining Si thickness substrate. The solid straight line represents the expected variation of n_s relative to in-plane biaxial strain ε_{xx} as calculated by equation (1).

The proposed method can be applied to a fully processed AlGaN/GaN HEMT wafer to increase the current density and reduce the access resistances in the devices: Figure 5 shows a comparison of the current-voltage characteristics of a standard HEMT, and the same device after etching 10% of its Si substrate thickness. The maximum current after Si etching is 27% higher than in the standard device. Moreover, higher on-current (i.e. lower R_{on}) is observed for the same low voltage in the linear region compared to the conventional AlGaN/GaN HEMTs. This new technology is currently being applied to increase the frequency performance of GaN HEMTs grown on Si substrates [3].

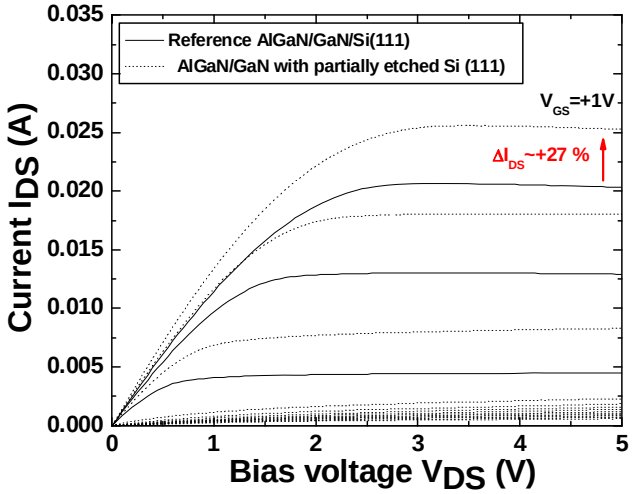
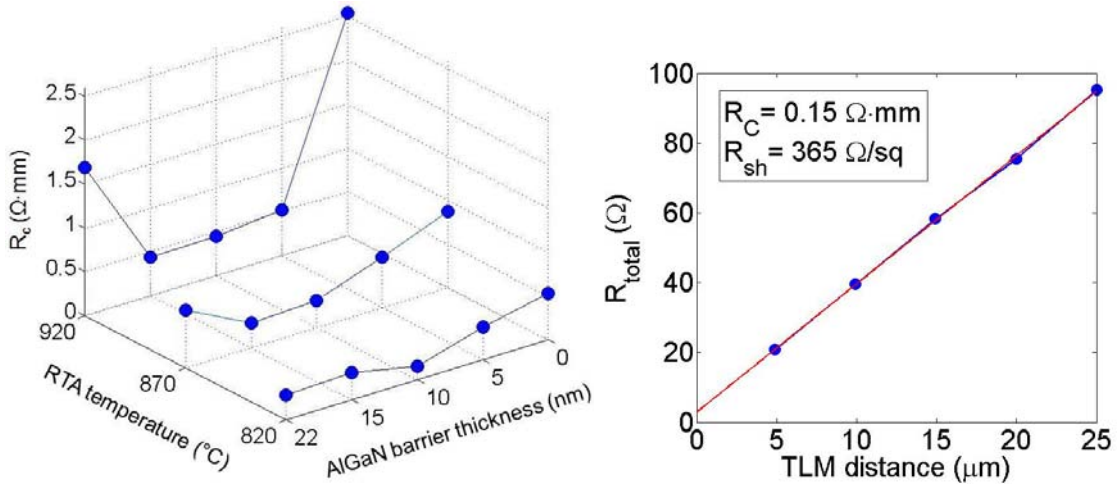


Figure 5: I-V characteristics of AlGaN/GaN transistors, before and after the partial removal of the Si substrate.

Task 2: New ohmic metal stack for ultra-low resistance

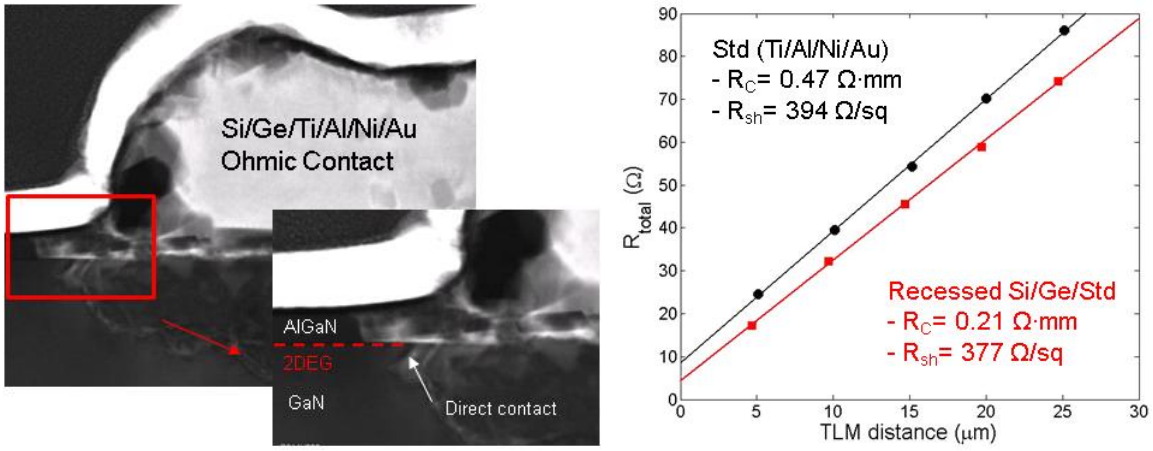
A new recessed ohmic technique was developed to reduce the ohmic contact resistances in GaN HEMTs. During the device fabrication, the source and drain regions were defined by photolithography and the AlGaN barrier was carefully recessed using a low power electron cyclotron resonance reactive ion etching (ECR-RIE) with Cl_2/BCl_3 gas mixture. To minimize the damage induced by ion bombardment, RF bias was kept low (~75 V) while ECR power was set to achieve an etch rate of 1 nm/min (~100 W). After the recess, a Ti/Al/Ni/Au metal stack was deposited, followed by rapid thermal annealing (RTA) for 30 sec in N_2 atmosphere. RTA temperature and remaining AlGaN barrier thickness were experimentally optimized to have the lowest contact resistance as shown in Figure 10. The best condition among the range we explored was found at 820°C with 10 nm AlGaN barrier yielding an R_c of 0.15 Ω·mm, which is one of the lowest contact resistances reported in the literature.



(a) (b)

Figure. 10. (a) Measured contact resistance (R_c) as function of RTA temperature and remaining AlGaN barrier thickness. (b) The optimum R_c of 0.15 Ω·mm was obtained at 10 nm AlGaN barrier after annealing at 820 °C for 30 s in N_2 ambient. The sheet resistance (R_{sh}) was kept almost constant (~365 Ω/sq) in all cases. In the devices with no remaining AlGaN barrier under the contacts, the ohmic contact is formed laterally between the annealed metals and the 2DEG in the unrecessed AlGaN/GaN access region.

In general, alloyed contacts have a very rough surface morphology and it reduces processing yield and reproducibility of numerous processing steps, especially the gate lithography for short source-to-drain distances (< 2 μm). To achieve both uniform surface and low contact resistance, a new recessed ohmic contact metallurgy based on alloyed Si/Ge/Ti/Al/Ni/Au (2/2/20/100/25/50 nm) contacts was developed (Figure 11). The new ohmic technology allowed us to reduce both ohmic contact resistance by 55 % (Figure 11) and surface roughness by 83 % (Figure 12) over conventional non-recessed Ti/Al/Ni/Au ohmic contacts.



(a) (b)

Figure 11. (a) Cross-section STEM image of recessed ohmic contact based on alloyed Si/Ge/Ti/Al/Ni/Au. (b) The contact resistance was reduced by 55% over conventional non-recessed Ti/Al/Ni/Au ohmic contacts.

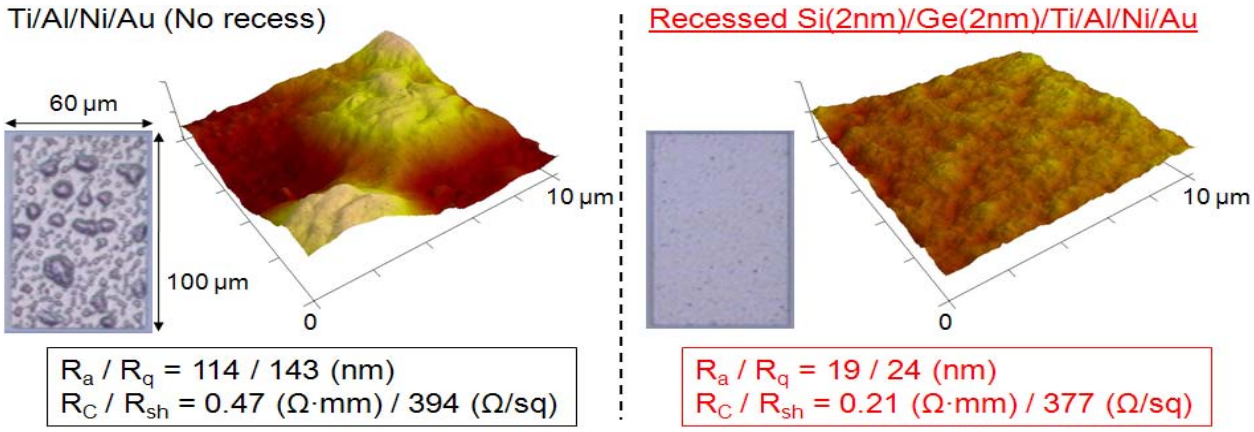


Figure 12. Comparison between conventional (left) and recessed Si(2nm)/Ge(2nm)/Ti/Al/Ni/Au ohmic contacts (right). Both of them were alloyed at 820 °C. 83% smoother surface roughness was observed for the new ohmic technology by AFM and microscopy images (inset).

Task 3: Advanced Recessed Ohmic Technology

Sufficiently low S/D resistance is necessary to obtain a low forward voltage drop in GaN transistors and to minimize the parasitic delays [5,6]. In addition, contact metallization containing Au suffers from rough surface morphology and it cannot be used in fabs shared with the fabrication of Si-based devices. In this project, we have developed two recess methods to reduce the contact resistances:

1- side-wall Au-based ohmic contact

2- Au-free ohmic contact

As shown in Figure 6, in our new technology the AlGaN barrier is completely removed underneath the ohmic contacts and the contact is performed laterally to the 2DEG in the channel region after a high temperature annealing.

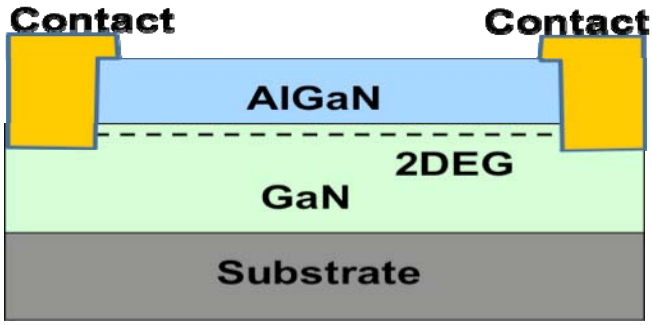


Figure 6: Side-wall metal contact of the 2DEG

Initial experiments were conducted on a standard 2 nm GaN/ 17.5 nm AlGaN/ 1 nm AlN/ 2 μm GaN / Si structures. Before depositing the ohmic metal stack of Ti (20nm) /Al (100nm) /Ni (25 nm) /Au (50 nm), a 40nm-deep recess was etched in the source and drain region using BCl_3/Cl_2. Then the ohmic metal was annealed at 870 ^oC for 30s. The transmission line method (TLM) measurements show a lower contact resistance of 0.6 Ω.mm (Figure 7), similar to the ohmic contacts in our conventional (unrecessed) AlGaN/GaN transistors.

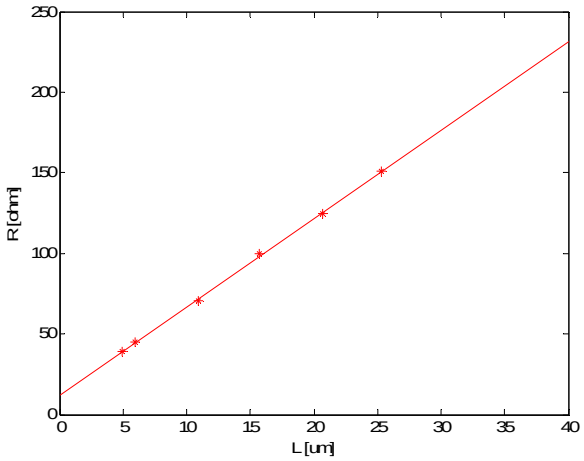


Figure 7: TLM of the sidewall ohmic contacts

Using this fully recessed-technology we have developed an Au-metallization scheme suitable to be used in Si-compatible fabs. A cross-sectional view of the fabricated TLM (Transmission Line Method) structure is shown in Figure 8.

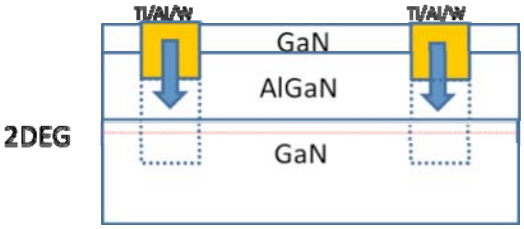


Figure 8: Schematic cross section of the fabricated GaN/AlGaN/GaN with recess.

In these devices, reactive ion etching (RIE) with a low power has been used to define surface recess and mesa structures. Structures with three different recess depths have been studied: ~5 nm (shallow etch), ~19 nm (medium etch), and ~30 nm (deep etch). AFM measurements have been done after each RIE etch to confirm the recess depth. Finally, a Ti/Al/W metallization was deposited by E-beam and then patterned by the lift-off method. The metal was annealed in a rapid thermal processing (RTP) chamber at 600–950 $^{\circ}$C, in nitrogen ambient. Current–voltage (*I*–*V*) measurements were performed using an HP4156 parameter analyzer on TLM structures to study contact behavior and extract contact resistances.

The contact resistance of GaN/AlGaN/GaN with different recess is deduced from TLM measurements and reported in Figure 9. For a shallow etch (~5 nm), the as-deposited contacts show a non-linear I-V characteristic, whereas the contacts changed to ohmic after annealing at 750 ˚C. The contact resistance is reduced down to ~6.5 Ω.mm by annealing at 850 ˚C. However, it increases again after 950 ˚C, reaching R_c ~10 Ω.mm. For a medium recess etch (~19 nm), to the contacts become ohmic contact after annealing them at 600 ˚C. In these devices, the contact resistance was been reduced to R_c ~6.6 Ω.mm at 700 ˚C. However, after 750 ˚C annealing the contacts become Schottky again. The best results were obtained for deep recess etches (~30 nm). These contacts show an ohmic behavior even as deposited, indicating good electron transfer to the AlGaN/GaN sidewall. After annealing at 870 ˚C, the contact resistance is dramatically reduced down to ~0.49 Ω.mm. This low contact resistance in a Au-free metallization is an important stepping stone for processing these devices in Si-compatible fabs.

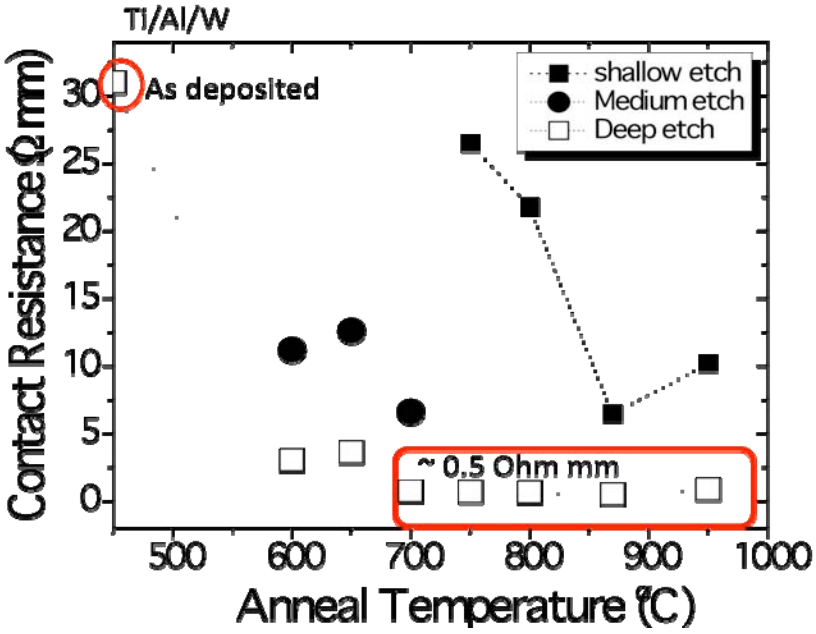


Figure . 9: Contact resistance as a function of anneal temperature for different recess depths. In all the cases, the ohmic metal is based on a Ti/Al/W stack.

Task 4: Nano-ribbon fabrication for reduced contact resistances

Nanowires (NWs) structures are very promising to minimize short channel effects in highly scaled transistors [7]. In addition, the NWs geometry allows to have a more intimate contact between the ohmic metal and the 2DEG at the interface of AlGaN/GaN structures, which (as we have shown in this project) reduces the contact resistances.

Recently, a transistor with 5 AlGaN/GaN NWs grown bottom-up by chemical vapor deposition has been demonstrated with promising RF performance (f_T ~5 GHz, f_{max}~12 GHz) [8]. However, the use of bottom-up-grown NWs in transistor structures remains technologically challenging due to the difficulty of aligning over the 1000's of them that are typically needed for providing enough current in power applications. The top-down fabrication of nano-ribbons-based (NRs) nitride HEMTs has a great potential to overcome those technological challenges [9]. Moreover, this top-down approach allows to integrate NRs and planar devices on the same chip and to make straightforward performance devices comparison.

In this work, we have fabricated lateral AlGaN/GaN NRs devices through a new top-down technology, which minimizes surface damage. The top-down fabrication of AlGaN/GaN NRs transistors is divided in two steps. First, the source and drain ohmic contacts are defined through optical lithography. A Ti/Al/Ni/Au metal stack was used for the ohmic metallization, followed by a 30 s anneal at 870ºC anneal as described in [10]. Arrays of AlGaN/GaN NRs were then patterned between the two ohmic contacts using electron-beam lithography. Reactive ion etching was used to etch away the material between adjacent nano-ribbons using a BCl_3 and Cl_2 chemistry [12]. A very slow etch rate (~ 0.9 nm/min) is used to minimize the surface damage on the sidewalls of the AlGaN/GaN NRs. The etch depth is 30 nm, as calibrated with a Veeco Dimension 3100 Atomic Force Microscope. The etch depth was deep enough to prevent electrical conduction between adjacent nano-ribbons. The inset of Figure 13 shows a typical Scanning Electron Microscopy (SEM) image of longitudinal AlGaN/GaN NRs fabricated using the technology previously described. The diameter (d) is varied from 70 to 145 nm and the pitch (or period) between nano-ribbons is p~140 nm. The width of nano-ribbons array is 100 μm. and the length of the nano-ribbons (L) is varied from 5 μm to 25 μm. Conventional planar devices with the same length and total width than the nano-ribbons were also fabricated on the same

wafer as a reference. Figure 13 shows the square resistance (R_{sq}) as extracted from transmission line method (TLM) measurements in the fabricated NRs devices. R_{sq} increases exponentially with reducing NRs diameter, which is in good agreement with the Refs 11 and 12. When the NRs diameter reaches d~70 nm, the R_{sh} is ~3.5 times higher than in planar device. This increase in R_{sh} in AlGaN/GaN NRs is expected since parts of AlGaN/GaN material have been removed in between NRs. As shown by Figure 14, the contact resistance (R_c) decreases when the NRs diameter is reduced and remains lower than for planar devices. This improvement of R_c can be explained by the higher ratio of contact region to nano-ribbons conduction channel. Negatives relatives values of R_c underlines that the absolute value of R_c in NRs is very low and as a consequence, reached the limit of the TLM method for very low R_c measurements.

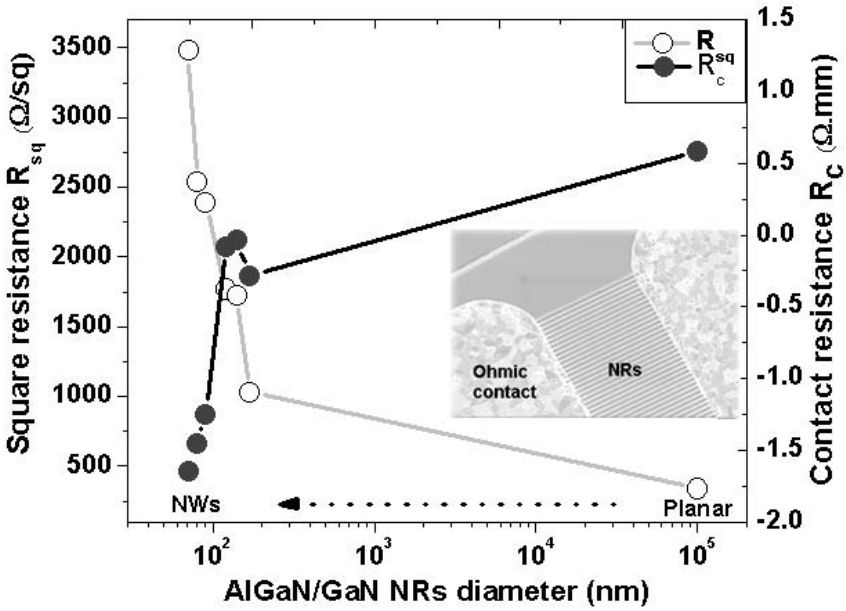


Figure 13: The inset is Scanning electron microscopy of AlGaN/GaN NRs between two ohmic contacts. The diameter and the pitch (periodicity) of the nano-ribbons are 70 nm and 170 nm, respectively. Square resistance (R_{sq}) and contact resistance (R_c) as function of NRs diameter

To get better understanding in the reduction of R_c in AlGaN/GaN NRs, Figure 14 reportes the R_c and the numbers of NRs as a function of the diameters. The reduction in R_c seems to be related to the increase of the number of NRs. The total resistance (R) (cf. inset of the Figure 14) in AlGaN/GaN NRs can be estimated to : $R= R_{sq} + 2R_c$/ Number of NRs, unlike in the

conventional planar device ($R= R_{sq} + 2R_c$). However, more work is currently being done to confirm this.

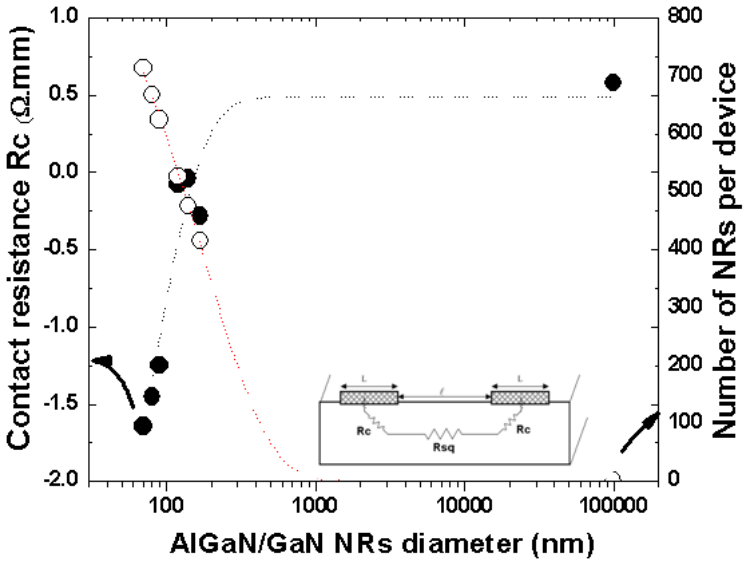


Figure 14: The inset is schematic of the total resistance in AlGaN/GaN device. Contact resistance (R_c) and the number of NRs per device as function of NRs diameter

Task 5: Si implantation of InAlN/GaN structures

The high sheet charge density of $In_{0.17}Al_{0.83}N$/GaN transistors and their reduced strain make these devices ideal for high power/high frequency application. Strong spontaneous polarization of the InAlN layer provides extremely high sheet charge density and makes it possible to achieve current density over 1.5 A/mm even with thin barrier, less than 10 nm thickness. In order to take advantage of the strength effectively and improve the device performance even further, reducing parasitic resistances is necessary. Moreover, considering the low sheet resistance of InAlN/GaN structures, the minimization of the contact resistance is one of the most important issues.

In our research, we introduced Si ion implantation to lattice-matched $In_{0.17}Al_{0.83}N$/GaN heterostructures for the first time in order to reduce parasitic resistances in InAlN/GaN HEMT. For process optimization, diverse factors such as implantation energy, implantation temperature, and annealing temperature are systematically investigated. In the sample implanted with 1 x 10^{15} cm^{-2} at 50 keV and annealed at 1300 °C, the sheet resistance of 98 Ω/ is obtained, which indicates more than 80 % dopant activation. Moreover, we developed a new advanced ohmic contact process combining ion implantation and barrier removal as shown in Figure 15, and an extremely low contact resistance of 0.04 Ω mm is achieved, the lowest ever reported in InAlN/GaN structures. Figures 16 and 17 shows the improvement of the contact resistance depending on each process step, and the TLM measurement results.

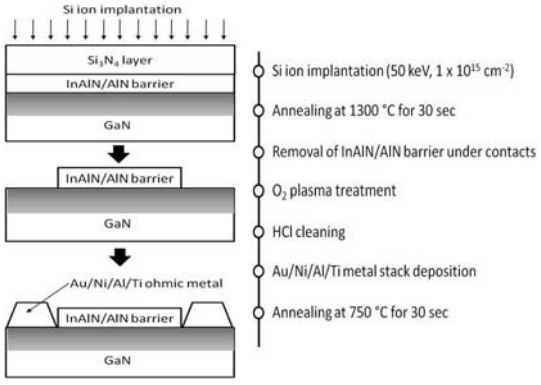


Figure 15. Advanced ohmic process flow.

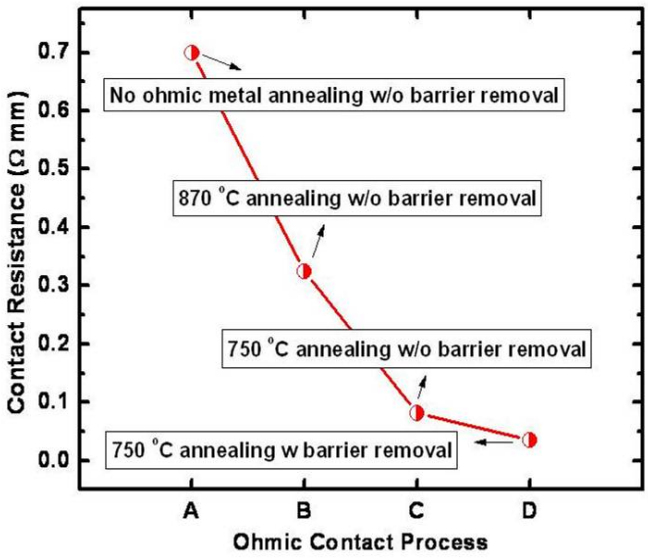


Figure 16. Improvement of the contact resistances depending on the each process step in the advanced ohmic process.

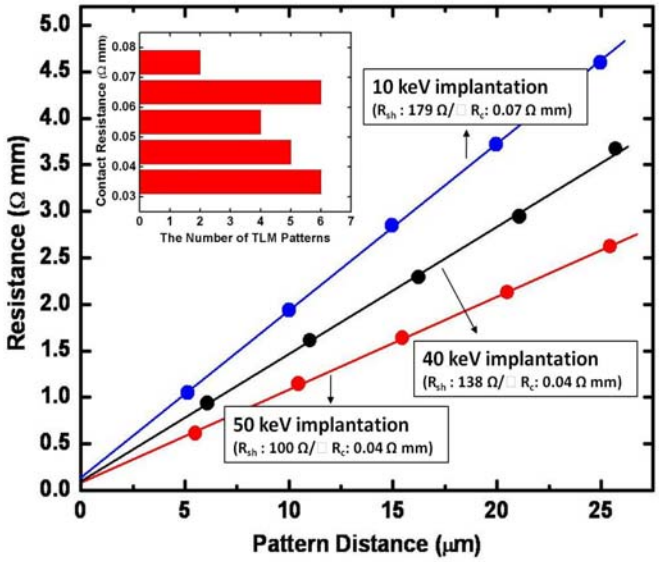


Figure 17. TLM measurement results of the samples implanted in the different energies. (inset: distribution of the contact resistance in the sample implanted in 50 keV).

Conclusion

In summary, during this project we have demonstrated five new approaches to reduce the access resistances in GaN HEMTs. This reduction in the access resistances is key to reduce the parasitic delays in GaN HEMTs and improve their frequency performance and efficiency.

As a first approach to reduce the access resistances in GaN HEMTs, additive tensile biaxial strain has been introduced into an AlGaN/GaN hetero-structure grown on a Si wafer by reducing the thickness of the Si substrate after the growth of the nitride epilayer. As a result, the electron sheet density increases by ~25% and reaches n_s~1x10^{13} cm^{-2}. As an example, the proposed substrate-etching technology has been used to increase the on-current in the linear region and the current density of AlGaN/GaN transistors grown on silicon by 27%.

In this project we have also developed different recessed ohmic technologies, which have allowed us to reduce R_c down to 0.15 Ω.mm, which is the lowest contact resistances reported in the AlGaN/GaN literature. To improve the surface roughness of the low contact resistance, a new ohmic metallization based on Si/Ge/Ti/Al/Ni/Au has been used and allowed us to reduce both ohmic contact resistance by 55 % and surface roughness by 83 % over conventional non-recessed Ti/Al/Ni/Au ohmic contacts. AlGaN/GaN nano-ribbons exhibit a lower R_c compared to the conventional planar device and seems promising for the next generation of AlGaN/GaN NRs transistors. Finally, Si implantation has also been used, for the first time in InAlN/GaN HEMTs, to achieve a low contact resistance of 0.04 Ω mm, which is the lowest ever reported in InAlN/GaN structures.

The development of these technologies has been key for the recent demonstration in our lab of AlGaN/GaN transistors with record frequency performance. Devices with an f_T of 225 GHz and an f_{max} of 300 GHz have been developed thank to the significant reduction of the parasitic delays achieved by these new technologies. Even better performance is expected in the future as the more advanced technologies, such as NR-based ohmic contacts and InAlN devices, mature. In addition, the development of a Au-free ohmic contact technology based on a Ti/Al/W metallization enables the fabrication of GaN-based transistors in Si fabs, an important stepping stone towards the on-wafer integration of these devices with Si electronics.

Finally, this project has also had a great impact on the ONR-sponsored Mm-wave Initiative for Nitride Electronics (MINE) MURI program. Details of this impact will be described in the final project report of the MINE MURI program.

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[Task 1]

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[Task 3]

J.W. Chung, T.W Kim and T. Palacios, "Advanced Gate Technologies for State-of-art f_T in AlGaN/GaN HEMTs", accepted to International Electron Devices Meeting, San Francisco, CA, 6-8 December 2010.

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[Task 4]

M.Azize, O.Saadat, H.Wang, B.Lu and T.Palacios "Top-down fabrication of InAlN/GaN nano-ribbons" International Workshop on Nitride Semiconductor, Tampa, FL, 19-24 September 2010.

M. Azize and T. Palacios, "Top-down fabrication of AlGaN/GaN Nano-ribbons," submitted to Appl. Phys. Lett, August 2010.

[Task 5]

D.S. Lee, M. Connor, C. Hatem, X. Guo and T. Palacios, "Ultralow Contact Resistance in InAlN/GaN Heterostructures Through Si Ion Implantation", International Workshop on Nitride Semiconductor 2010, Tampa, FL, 19-24 September 2010.